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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,852	03/02/2004	Karsten Wieczorek	2000.110600	3105

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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,852	WIECZOREK ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/15/04 & 11/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9-18 and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al. (U.S. Patent No. 6,252,277). With regard to Claim 1, Chan discloses a method of forming a field effect transistor (column, lines 4-6), the method comprising:

forming (column 4, lines 39-51) an implantation mask (32, 37) over a crystalline semiconductor region;

forming a drain region and a source region (39) using said implantation mask (column 5, lines 7-17), said drain and source regions each having a top surface located above a surface of said crystalline semiconductor region (figure 4E);

removing said implantation mask to expose a surface area of said crystalline semiconductor region (column 5, lines 18-24);

forming a gate insulation layer (44) on said exposed surface area (column 5, lines 57-59);

forming a gate electrode (47), out of polysilicon layer (46), on said gate insulation layer (column 6, lines 22-24); and

doping said gate electrode (column 5, lines 66-67 and column 6, lines 1-3).

With regard to Claim 2, Chan discloses forming a gate electrode (47) including depositing a gate electrode material (column 5, lines 61-63) above a gate insulation layer (44) and removing excess material of said gate electrode to form the gate electrode (column 6, lines 8-12).

With regard to Claim 3, Chan discloses a lateral size of the implantation mask (32, 37) that greater than a design value (figures 4B, 4F and 4I) of a gate length of the gate electrode (47).

With regard to Claim 4, Chan discloses forming drain and source regions (39) including epitaxially-growing (column 5, lines 7-17) a crystalline semiconductor layer adjacent to (figure 4E) an implantation mask (32, 37).

With regard to Claim 5, Chan discloses a first implantation sequence for forming said drain and source regions is performed prior to epitaxially-growing the semiconductor layer and a second implantation sequence for forming said drain and source regions is performed after epitaxially-growing the semiconductor layer (column 5, lines 7-17 and lines 34-40).

With regard to Claim 9, Chan discloses forming sidewall spacers (35) on sidewalls of the drain and source regions (column 5, lines 10-13) that are exposed by removing an implantation mask (32, 37).

With regard to Claim 10, Chan discloses a width of sidewalls spacers (35) controlled on the basis of target length (figure 4B) for a gate electrode (47).

With regard to Claim 11, Chan discloses an implantation mask (32, 37) that is removed by an isotropic-etch process (column 5, lines 51-54).

With regard to Claim 12, Chan discloses removing an excess material (46) to form a gate electrode (47), by chemical-mechanical polishing (column 6, lines 8-9).

With regard to Claim 13, Chan discloses removing an excess material (46) to form a gate electrode (47), by an etch-process (column 6, lines 9-10).

With regard to Claim 14, Chan discloses removing an excess material (46) to form a gate electrode (47), by chemical-mechanical polishing (column 6, lines 8-9) and an etch-process (column 6, lines 9-10).

With regard to Claim 15, Chan discloses forming metal/semiconductor compound regions (column 6, lines 29-32) on the gate electrode (47) and drain and source regions (39).

With regard to Claim 16, Chan discloses forming said implantation mask includes forming a recess in a semiconductor layer including said crystalline semiconductor region and filling said recess with a mask material to form said implantation mask (figures 4A-4F).

With regard to Claim 17, Chan discloses filling said recess includes depositing said mask material with a thickness that is sufficient to completely fill said recess, and removing excess material by chemical mechanical polishing (column 4, lines 44-49).

With regard to Claim 18, Chan discloses a lateral dimension of a recess that is greater than a target length (figures 4B and 4I) of a gate electrode (47).

With regard to Claim 21, Chan discloses doping of the gate electrode that is performed on the basis of process parameters selected to restrict dopant-penetration of the gate insulation layer (column 5, lines 57-67 and column 6, lines 1-3).

With regard to Claim 22, Chan discloses a field-effect transistor (column, lines 4-6), comprising:

a substrate (30) having formed thereon a semiconductor region;

a drain region (39) extending along a lateral direction and a height direction (figure 4E);

a source region (39) extending along a lateral direction and a height direction (figure 4E);

a gate electrode (47) extending along said lateral direction and said height direction said gate electrode laterally located between said drain region and said source region and separated from said semiconductor region by a gate insulation layer (44), said drain and source regions extending along said height direction at least to an upper surface of said gate electrode (figure 4E).

With regard to Claim 23, Chan discloses a gate electrode (47) that is partially-comprised of a doped semiconductor material (column 5, lines 67-68 and column 6, lines 1-3); whereby a peak concentration of dopants in said gate electrode is less than a peak concentration of dopants in said drain and source regions (column 5, lines 13-15).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8, 19, 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 6,252,277) in view of Gardner et al. (U.S. Patent No. 6,355,955). With regard to Claim 6, Chan essentially discloses the claimed invention but fails to show the step of performing an anneal process to activate dopants.

However, Gardner discloses a method for forming a transistor, including an anneal process to activate dopants (column 12, lines 40-41). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include the step of performing an anneal process to activate the dopants, as suggested by Gardner, in order to enhance the implantation process by effectively activating impurities and positioning these in a semiconductor region (column 12, lines 40-41).

With regard to Claim 7, a further difference between the claimed invention and Chan is, an anneal process is controlled on the basis of a desired channel length defined by a lateral distance of the drain region and the source region.

However, Gardner discloses an anneal process is controlled on the basis of a desired channel length defined by a lateral distance of the drain region and the source region (column 12, lines 26-40). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include the step of an anneal process is controlled on the basis of a desired channel length defined by a lateral distance of the drain region and the source region, as suggested by Gardner, in order to enhance the implantation process by effectively introducing and activating impurities in a semiconductor region to create active regions.

With regard to Claim 8, Chan discloses a first implantation sequence for forming said drain and source regions is performed prior to epitaxially growing the semiconductor layer and a second implantation sequence for forming said drain and source regions is performed after epitaxially growing the semiconductor layer (column 5, lines 7-17 and lines 34-40).

Chan fails to disclose the claimed anneal process. However, Gardner discloses a method for forming a transistor, including an anneal process to activate dopants (column 12, lines 40-41). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include the step of performing an

anneal process to activate the dopants, as suggested by Gardner, in order to enhance the implantation process by effectively activating impurities and positioning these in a semiconductor region (column 12, lines 40-41).

With regard to Claim 19, Chan essentially discloses the claimed invention but fails to disclose, a recess formed by anisotropically etching a semiconductor layer.

However, Gardner discloses a method for forming a transistor including an anisotropic etch process on a semiconductor layer (column 12, lines 36-38). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include the claimed recess formed by anisotropically etching a semiconductor layer, in order to reduce the distance between an upper surface of a silicon substrate and the lower surface of a gate conductor (column 12, lines 38-41).

With regard to Claim 20, a further difference between the claimed invention and Chan is, an anisotropic etch process that is controlled on the basis of an initial thickness of said semiconductor layer so as to obtain a depth of said crystalline region in conformity with a predefined target value.

However, Gardner discloses a method for forming a transistor including an anisotropic etch process on a semiconductor layer (column 12, lines 36-38). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the

method as disclosed by Chan to include the claimed anisotropic etch process that is controlled on the basis of an initial thickness of said semiconductor layer so as to obtain a depth of said crystalline region in conformity with a predefined target value, in order to reduce the distance between an upper surface of a silicon substrate and the lower surface of a gate conductor (column 12, lines 38-41).

With regard to Claim 24, a further difference between the claimed invention and Chan is, the claimed semiconductor region formed on an insulating layer and having an extension in the height direction in the range of approximately 5-50 nm.

However, Gardner discloses a height of a semiconductor layer that can be modified (column 12, lines 36-54), therefore it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include the claimed height, in order to minimize diffusion of impurities into the channel region (column 12, lines 50-54). Additionally, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. Regarding the claimed insulating layer, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Chan to include a semiconductor region formed on an insulating layer, in order to provide an insulating layer for semiconductor device such as a thin-film transistor (TFT).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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